Tipos de datos sintetizables y sus paquetes [1]

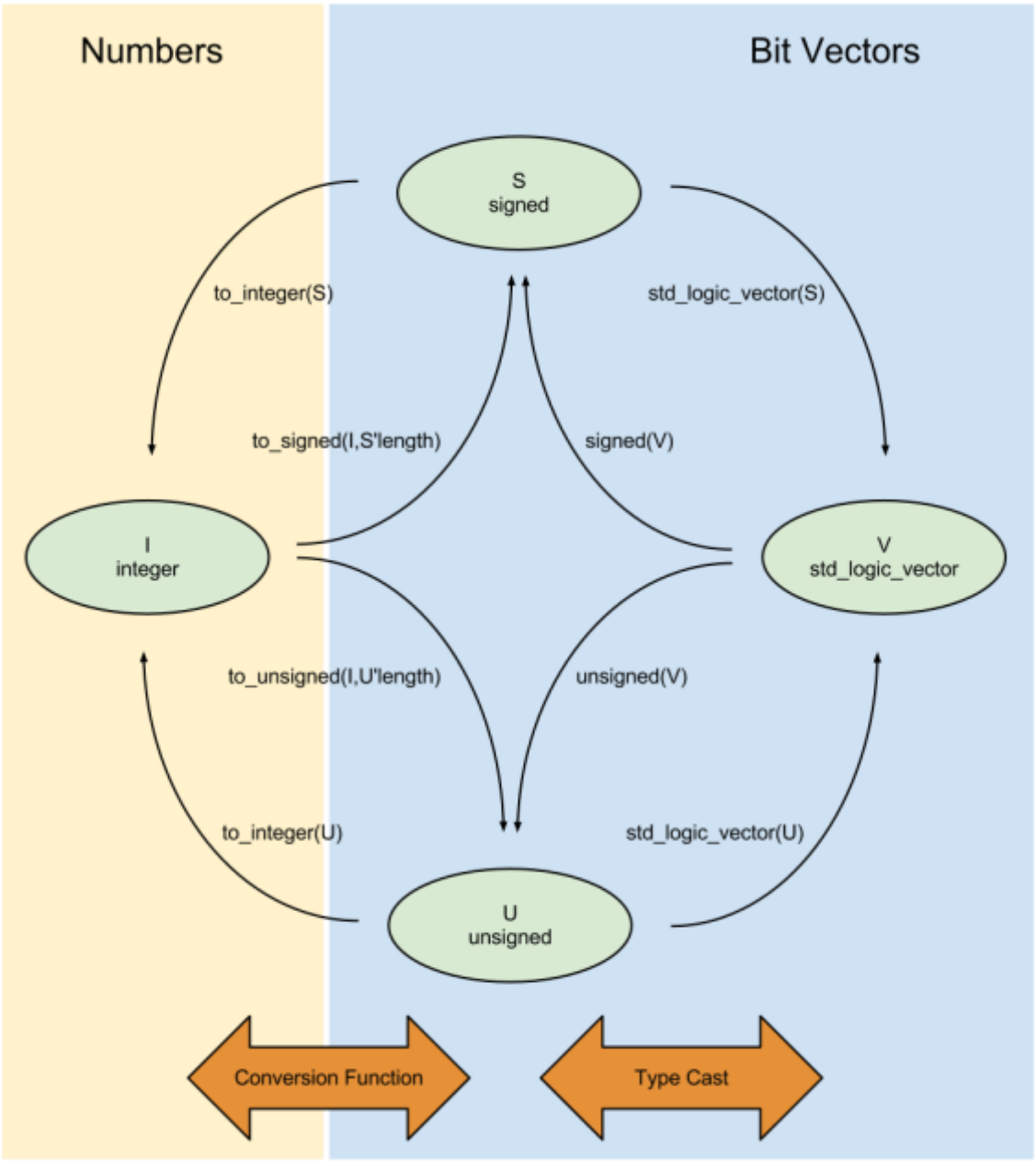
Category	Package of origin	Predefined synthesizable types	Dimension
Standard	standard	BIT	Scalar
		BIT_VECTOR	1D
		BOOLEAN	Scalar
		INTEGER	1D
		NATURAL	1D
		POSITIVE	1D
		CHARACTER	1D
		STRING	1Dx1D
	standard (2008 expansion)	BOOLEAN_VECTOR	1D
		INTEGER_VECTOR	1DX1D
	numeric_bit_unsigned (2008)	(only operators for BIT and BV)	---
Standard logic	std_logic_1164	STD_(U)LOGIC	Scalar
		STD_(U)LOGIC_VECTOR	1D
	std_logic_1164 (2008 expansion)	STD_(U)LOGIC	Scalar
		STD_(U)LOGIC_VECTOR	1D
	std_logic_unsigned	(only operators for SLV)	---
	std_logic_signed	(only operators for SLV)	---
	numeric_std_unsigned (2008)	(only operators for SL and SLV)	---
Unsigned and Signed	numeric_bit	UNSIGNED (base=BIT)	1D
		SIGNED (base=BIT)	1D
	numeric_std	UNSIGNED (base=STD_LOGIC)	1D
		SIGNED (base=STD_LOGIC)	1D
	std_logic_arith	UNSIGNED (base=STD_LOGIC)	1D
		SIGNED (base=STD_LOGIC)	1D
Fixed and Floating point	fixed_pkg + associated packages (2008)	UFIXED	1D
		SFIXED	1D
	float_pkg + assoc. pack. (2008)	FLOAT	1D

Conversiones de tipos [1]

From	To	Type conversion function	Package of origin
INTEGER	STD_LOGIC_VECTOR	conv_std_logic_vector(a, cs)	std_logic_arith
	UNSIGNED	to_unsigned(a, cs) conv_unsigned(a, cs)	numeric_std std_logic_arith
	SIGNED	to_signed(a, cs) conv_signed(a, cs)	numeric_std std_logic_arith
	UFIXED	to_ufixed(a, cs)	fixed_generic_pkg
	SFIXED	to_sfixed(a, cs)	fixed_generic_pkg
	FLOAT	to_float(a, cs)	float_generic_pkg
BIT_VECTOR	STD_LOGIC_VECTOR	to_stdlogicvector(a, cs)	std_logic_1164
STD_LOGIC_VECTOR	INTEGER	conv_integer(a, cs) conv_integer(a, cs) to_integer(a, cs)	std_logic_signed std_logic_unsigned numeric_std_unsigned
	BIT_VECTOR	to_bitvector(a, cs)	std_logic_1164
	UNSIGNED	unsigned(a) (*) unsigned(a) (*)	numeric_std std_logic_arith
	SIGNED	signed(a) (*) signed(a) (*)	numeric_std std_logic_arith
	UFIXED	to_ufixed(a, cs)	fixed_generic_pkg
	SFIXED	to_sfixed(a, cs)	fixed_generic_pkg
	FLOAT	to_float(a, cs)	float_generic_pkg
UNSIGNED and SIGNED	INTEGER	to_integer(a, cs) conv_integer(a, cs)	numeric_std std_logic_arith
	STD_LOGIC_VECTOR	std_logic_vector(a) (*) std_logic_vector(a) (*) conv_std_logic_vector(a, cs)	numeric_std std_logic_arith std_logic_arith
	UNSIGNED	conv_unsigned(a, cs)	std_logic_arith
	SIGNED	conv_signed(a, cs)	std_logic_arith
	UFIXED (unsigned only)	to_ufixed(a, cs)	fixed_generic_pkg
	SFIXED (signed only)	to_sfixed(a, cs)	fixed_generic_pkg
	FLOAT	to_float(a, cs)	float_generic_pkg
UFIXED and SFIXED	INTEGER	to_integer(a, cs)	fixed_generic_pkg
	STD_LOGIC_VECTOR	to_slv(a, cs)	fixed_generic_pkg
	UNSIGNED (ufixed only)	to_unsigned(a, cs)	fixed_generic_pkg
	SIGNED (sfixed only)	to_signed(a, cs)	fixed_generic_pkg
	SFIXED (ufixed only)	to_sfixed(a, cs)	fixed_generic_pkg
	FLOAT	to_float(a, cs)	float_generic_pkg
FLOAT	INTEGER	to_integer(a, cs)	float_generic_pkg
	STD_LOGIC_VECTOR	to_slv(a, cs)	float_generic_pkg
	UNSIGNED	to_unsigned(a, cs)	float_generic_pkg
	SIGNED	to_signed(a, cs)	float_generic_pkg
	UFIXED	to_ufixed(a, cs)	float_generic_pkg
	SFIXED	to_sfixed(a, cs)	float_generic_pkg

(a, cs) = (argument, conversion specifications)
cs may include vector size, left/right range constants, overflow and rounding specs, etc. (consult package)
(*) = type casting

Figura sobre conversiones de tipos [2]



Referencias

[1] Circuit Design with VHDL, V. Pedroni, The MIT Press, 2010.

[2] https://forums.xilinx.com/t5/7-Series-FPGAs/About-TO-SIGNED-function/td-p/646308